

# PROSPECTS OF SILICON NANO-ELECTRONICS

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## Abstract

*Silicon technology and nanoelectronics are two important components which will shape the future of the IC industry. This paper discusses their mutual interaction, i.e. the contribution that nanotechnology may offer to the evolution of MOS processing, as well as the role that silicon technology could play in the projected development of nanoelectronic circuits.*

## 1 Introduction

The latest version of the SIA roadmap, published in 1994 [1], has triggered a conceptual breakthrough by introducing for the first time the prospect of nanoelectronics in the strategic planning of the microelectronics industry. Indeed, notwithstanding the scepticism of some observers, the SIA is confident that the IC trends will continue to obey Moore's law until the year 2010, leading to MOS transistors with  $0.07\ \mu\text{m}$  (i.e. "nano" scale) gate lengths (a new version of the roadmap, due later this year, will probably be even more aggressive). After this date there is a general feeling that evolutionary strategies based on Moore-like projections will gradually run out of power, leaving room for several - mostly divergent - alternatives. A major difficulty in forecasting such matters arises from the fact that some technologies are essentially scale-bounded, whereas others only define scaling limits in a relative sense. For example, there can be no doubt that, with shrinking dimensions, a MOS transistor will ultimately cease to operate as a proper field-effect device [2]. Although the scale at which this will practically happen may be debatable, the existence of well-defined physical limits to transistor operation is an unavoidable fact. On the other hand, the technical limit to interconnect complexity is much harder to define. Adding layer upon layer of wiring will prove increasingly impractical, but the burden could be shifted to other areas e.g. by placing some interconnect levels on the package substrate or developing novel schemes for circuit architecture and / or lay-out [3].

## 2 Nanoelectronics along the roadmap

Ever since the pioneering work of Sai-Halasz et al. [4], the physics of sub- $0.1\ \mu\text{m}$  devices has been under close investigation. Particular attention has been given to the possible occurrence of new physics such as ballistic transport, tunneling effects or quantum interference. Evidence for ballistic behaviour of electrons comes mainly from Monte-Carlo simulations e.g. of 30 nm channel length devices with dual gate geometry [5]. The experimental picture is less clear, as the observation of velocity overshoot strongly depends on biasing conditions [6]. Tunneling-dominated operation has been observed by Harstein in

the I-V characteristics of sub- $0.01\mu\text{m}$  (!) devices [2] which can hardly be called field-effect transistors. Quantum interference effects seem to be limited to quantum wire devices operating at very low temperature [7]. The generally accepted picture of a nanoscale MOSFET is presently that of a classical device with increased  $V_T$  fluctuations and sub-threshold leakage as the main performance limiting factors [8]. For this reason, we face the paradoxical situation that the most promising nanoelectronic device has in fact drawn very little attention from the nanoelectronics research groups ! However, this situation may change as new design concepts propose to change rather drastically the geometry of these transistors in the future. Introducing both SiGe epitaxial structures and vertically etched channels will bring both the structure and the physics of ultra-small MOSFETs closer to a well-known nanoelectronic paradigm such as the quantum dot [9]. SiGe quantum dots are currently investigated, both for optical and for switching applications [10]. Some of the background information already available should be of interest to advanced MOSFET designers, especially concerning the link between carrier transport and device technology.

Further on the processing side, we may expect a gradual intake of nanotechnology features into three areas of mainstream IC fabrication nl. deposition, lithography and dry etching. However, in most cases this influence should be inspirational rather than based on direct transfer. For example, the favourite epitaxial technique in nanoelectronic research is MBE, but in IC fabrication CVD methods are preferred, both for higher throughput and larger wafer sizes. The materials background however remains the same, and the available expertise should be of use to future process developers. In lithography, the situation is more complex and has recently been reviewed by Broers [11]. E-beam direct write is the most popular nanolithography technique, but in spite of several ongoing efforts [12-14], it still lacks a high throughput approach suitable for large-scale manufacturing. For the same reasons, Scanning Probe Lithography remains on the far future horizon, although the technique is finding a short term niche as an advanced imaging and metrology tool [15]. In dry etching, the micro- and nanoelectronics practices are closely similar. There is a common equipment base and most processes only require limited tuning to geometry and scaling conditions. However, mesoscopic structures usually involve substrate etching only, which up to now has not been a critical issue in IC processing. This may change since the introduction of vertical geometries will put Si and SiGe patterning in a central perspective, making the available experience (especially on the limitation of etch damage) even more relevant.

At the packaging level, a shift to cryogenic temperatures has become a serious issue since ultra-small MOSFETs will exhibit unacceptable room temperature dissipation currents in the off-state due to subthreshold leakage [16]. Operation at low temperatures is a common feature of most nanoelectronic devices, and considerable experience on this matter is already available. However, the cryogenic option may limit the use of the nano-MOSFET technology to large-scale systems with integrated cooling units, unless progress in microcooling tools and cryopackages would allow inexpensive cooling at the chip level.

### **3 Nanoelectronic devices off the road**

Turning to a broader scene, one might wonder what role silicon could play in the hypothetical quantum age which is supposed to dawn after the CMOS roadster will have reached

the end of its journey. The tentative answer is that silicon has also the best chances of becoming the semiconductor material of the nano-world. Indeed, although the latter has been traditionally a stronghold of III-V compounds, there are today numerous examples of nanostructures based on Si-related materials [17]. Recent technical developments including SiGe heterojunctions as well as various kinds of nanocrystalline silicon (cfr. porous silicon !) have greatly extended the scope of thinkable applications. Both SiGe/Si and SiO<sub>2</sub>/Si interfaces can be used for quantum well and superlattice formation, and in this context they also play a central role in the search for light emitting silicon structures [18, 19]. With respect to logic and memory circuits, silicon is already the favourite material candidate for single electron devices and may also provide a technological base for future resonant tunneling circuits.

### 3.1 Single electron transistors (SET)

Any electron device, whatever its material or architecture, will become sensitive to single electron charging effects when scaled down to sufficiently small dimension. Coulomb blockade is indeed a thermodynamic effect depending on the ratio of the charging energy of the device vs.  $kT$ . The first successful single electron semiconductor device operating at room temperature was essentially a MOS transistor containing oxide coated nanocrystalline Si grains deposited by CVD [20]. However, the present poly-Si technology is impractical for SET circuit fabrication because of large size fluctuations in the deposited crystallites. Several techniques are under development which could in principle deliver much more uniform particle sizes, e.g. by using size filtering set-ups or size-selected precipitation [21]. The only lithographic alternative which could produce room temperature devices is the Scanning Probe Lithography for patterning the conduction islands and tunneling barriers. This has indeed been attempted, e.g. using anodic oxidation of titanium with an STM tip to create a 30 nm × 35 nm Ti island isolated by TiO<sub>x</sub> barriers on a SiO<sub>2</sub>/Si substrate [22].

The future of SETs is still an open question. The scale of the devices presently available for logic or memory circuits requires their cooling to liquid helium temperature or lower. Although higher temperatures could in principle become practical by further downscaling, it has been questioned on theoretical grounds whether room temperature operation may be possible at all [23]. Moreover, the very nature of correlated single electron tunneling requires isolation barriers around the islands to be on the order of the quantum resistance (25kΩ), making those devices rather slow for switching applications. In addition, the SET has very little gain, making it difficult to interface with the outer world. Therefore, the most realistic strategy, providing the huge technological difficulties can be overcome, would be to use the SETs for multi-terabit memory elements in combination with MOS read/write circuitry.

### 3.2 Resonant tunneling devices

Although the description of correlated single electron tunneling makes use of standard quantum tunneling theory, the main feature of this effect is that of charge quantization, so that it still belongs to the "pre-Schrödinger" era. On the other hand, many other devices have been proposed and some even put to work by exploiting genuine wave-mechanical features of the electron. They now form a set which is often dubbed as

"quantum functional devices". The most mature of these components is the resonant tunnelling diode (RTD), which through the years has given rise to an important field of research in mesoscopic physics. The RTD offers promises for very high frequency current sources as well as for compact memory/logic cells due to its multistability. Another asset of this device is its potential to operate at room temperature without the need for nanoscale patterning. Like all two-terminal devices however, its major disadvantage is the lack of signal regeneration. A combination of RTDs with classical transistors such as MOSFETs or MODFETs is therefore desirable to increase the fan-out.

Most of the work on RTD's is based on III-V materials, but the possibility to use Si-based epitaxial layers has also been demonstrated [24]. At this point however, there is a large gap between the GaAs based technology, in which a variety of circuit demonstrators have been produced going from SRAM cells to logic gates, and the SiGe realizations which are still limited to individual devices. The main problem for logic applications is the strain management [25], since high Ge concentrations (up to 40% increase the tunneling barrier height sufficiently for RT operation. This would require new developments in the so-called "virtual substrate" technology or else one may have to satisfy oneself with 77K operation. Moreover, the realization of large-scale circuits is stumbling against the extremely tight geometrical control which is required to limit the spread of electrical parameters, especially  $V_T$ . With respect to memory applications, the prospects for RT memory circuits based on SiGe RTDs are definitely better than with SETs.

### 3.3 Other devices

Another class of devices which has recently attracted some interest, especially in Japan, is that of quantum interference devices. These components rely on the phase coherence of electron waves when travelling ballistically through a mesoscopic conduction channel. Controlling the interference condition (constructive or destructive) using e.g. the Aharonov-Bohm effect should allow to emulate transistor switching with unrivalled power/delay products [26]. Quantum interference has indeed been detected in low-dimensional structures fabricated on III-V heterojunction substrates [27]. More recently, the observation of Aharonov-Bohm effects in Si/ SiGe structures has also been reported [28]. To achieve ballistic transport over mesoscopic distances, cooling to very low temperatures (typically below 4K) is required in order to suppress inelastic phonon scattering. For this reason, device concepts based on quantum interference have not been very popular in the West and their prospects for industrial implementation are virtually non-existent.

## 4 A European roadmap for nanoelectronics ?

The spectacular advances of nanotechnology together with the strong prospective push created by the latest versions of the SIA roadmap has created a climate of uncertainty over the long-term future of microelectronics. If the technological endpoint of CMOS will indeed be reached within the next 15 - 20 years, what will come next ? There is a general feeling that more action is needed to shape the future, and that the time to act has come now. It is therefore not surprising that new nanoelectronics initiatives have recently been launched in the three major industrial areas of the world. In Europe, the ESPRIT Long Term Research programme is now hosting the so-called "Advanced Research Initiative"

on microelectronics. This action consists of five projects in the optoelectronics and nine projects in the nanoelectronics field (more information can be found on the ESPRIT website). Projects in each branch are clustered to improve coherence and cross-linking between the individual consortia. It is interesting to notice that MOS is the single technology most frequently represented in the nanoelectronics cluster, where it will be compared with alternatives based on molecular electronics, magnetic materials and superconductive devices. The programme should also result in the proposal of a European Roadmap for nanoelectronics, which will evaluate the prospectives offered by the various technologies on a tentative timescale.

Whatever its final version will be, it is clear that the new roadmap must consider the possibility that the future of electronics may not belong entirely to the semiconductor family. This, in fact, is not a new situation. After all, vacuum tubes have already shown us a long time ago that the basic electronic material need not be a semiconductor! Since none of the presently available nano-components seems to offer the same promise of universality that CMOS is now enjoying, we may end up with a set of niches in which dedicated technologies will perform specific functions for which they are best suited. Providing, of course, that this specialization would not contradict the universal laws of industrial economics . . .

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